AMENDMENTS TO THE CLAIMS

Claims 1-7 (Cancelled)

8. (Currently Amended) A method, comprising:

speculatively allocating a first branch entry for a conditional branch in a speculative branch target buffer (SBTB) prior to execution of the conditional branch responsive to decoding the conditional branch and finding no branch entry in an architectural branch target buffer (ABTB) corresponding to the conditional branch, wherein the SBTB and the ABTB are included in a branch target buffer (BTB) to eliminate the speculative history from the ABTB;

speculatively allocating a second branch entry for the conditional branch in the SBTB responsive to a subsequent failed attempt to locate a branch entry in the ABTB corresponding to the conditional branch;

allocating a third branch entry for the conditional branch in the ABTB after retirement of the conditional branch; and

subsequently performing branch prediction for the conditional branch by determining a predicted target address branch based upon branch data associated with the second branch entry.

9. (Previously Presented) The method of claim 8, further comprising speculatively updating branch data associated with the first branch entry after said performing branch prediction for the conditional branch.

Claims 10-13 (Cancelled)

14. (Currently Amended) A machine-readable medium having stored thereon data representing sets of instructions, the sets of instructions which, when executed by a machine, cause the machine to:

speculatively allocate a first branch entry for a conditional branch in a speculative branch target buffer (SBTB) prior to execution of the conditional branch responsive to decoding the conditional branch and finding no branch entry in an architectural branch target buffer (ABTB) corresponding to the conditional branch, wherein the SBTB and the ABTB are included in a branch target buffer (BTB) to eliminate a speculative history from the ABTB;

speculatively allocate a second branch entry for the conditional branch in the SBTB responsive to a subsequent failed attempt to locate a branch entry in the ABTB corresponding to the conditional branch;

allocate a third branch entry for the conditional branch in the ABTB after retirement of the conditional branch; and

subsequently perform branch prediction for the conditional branch by determining a predicted target address branch based upon branch data associated with the second branch entry.

15. (Previously Presented) The machine-readable medium of claim 14, wherein the sets of instructions which, when executed by the machine, further cause the machine to speculatively update branch data associated with the first branch entry after said performing branch prediction for the conditional branch.

Claims 16-20 (Cancelled)

21. (Currently Amended) A processor, comprising:

a fetch unit to speculatively retrieve instruction data for processing by an instruction pipeline; and

a branch prediction circuit, coupled to the fetch unit, to predict final target addresses for branch instructions contained within the instruction data, the branch prediction circuit including

a branch target buffer (BTB), the BTB having

a speculative branch target buffer (SBTB) cache having a plurality of branch entries to maintain speculative branch data associated with in-flight branches, the speculative branch data including a speculative history of taken/not-taken outcomes associated with the in-flight branches, and

an architectural branch target buffer (ABTB) cache, coupled to the SBTB cache, the ABTB having a plurality of branch entries to maintain architectural branch data including the actual taken/not-taken outcomes associated with retired conditional branches, wherein the SBTB and ABTB are included in the BTB to eliminate the speculative history from the ABTB.

22. (Previously Presented) The processor of claim 21, wherein the SBTB cache comprises a FIFO having entries corresponding to each of a plurality of pipeline stages of the instruction pipeline.

23. (Previously Presented) The method of claim 9, wherein the branch data includes a

speculative history field representing the speculative taken or not-taken history of the branch for a predetermined window of executions of the branch, and wherein said speculatively updating branch data comprises updating the speculative history field to reflect the taken or not-taken status of its most recent execution.

24. (Previously Presented) The machine-readable medium of claim 15, wherein the branch data includes a speculative history field representing the speculative taken or not-taken history of the branch for a predetermined window of executions of the branch, and wherein said speculatively updating branch data comprises updating the speculative history field to reflect the taken or not-taken status of its most recent execution.

25. (Previously Presented) The processor of claim 21, wherein the SBTB cache comprises a dual-ported SBTB cache.

26. (Previously Presented) The processor of claim 21, wherein the SBTB cache comprises a single-ported SBTB cache.

27. (Previously Presented) The processor of claim 21, wherein the ABTB cache comprises a single-ported ABTB cache.

28. (Currently Amended) A branch prediction circuit, comprising:

a branch target buffer (BTB), the BTB having

a speculative branch target buffer (SBTB) cache having a plurality of branch entries to maintain speculative branch data associated with in-flight branches, the speculative branch data including a speculative history of taken/not-taken outcomes associated with the in-flight branches, wherein the SBTB cache includes a FIFO

having entries corresponding to each of a plurality of pipeline stages of a processor instruction pipeline, and

an architectural branch target buffer (ABTB) cache coupled to the SBTB cache, the ABTB cache having a plurality of branch entries to maintain architectural branch data including actual taken/not-taken outcomes associated with retired conditional branches, wherein the SBTB and ABTB are included in the BTB to eliminate the speculative history from the ABTB; and

a target address generator coupled to the BTB, the target address generator to determine a predicted target address for a branch prediction based upon the speculative branch data and the architectural branch data.

29. (Previously Presented) The branch prediction circuit of claim 28, further comprises a fetch unit to speculatively retrieve instruction data for processing by the processor instruction pipeline.

30. (Previously Presented) The branch prediction circuit of claim 28, wherein the SBTB cache comprises a dual-ported cache.

31. (Previously Presented) The branch prediction circuit of claim 28, wherein the SBTB cache comprises a single-ported cache.

32. (Previously Presented) The branch prediction circuit of claim 28, wherein the ABTB cache comprises a single-ported cache.

33. (Currently Amended) A method, comprising:

maintaining speculative branch data associated with in-flight branches using a speculative branch target buffer (SBTB) cache having a plurality of branch entries, the speculative branch data including a speculative history of

taken/not-taken outcomes associated with the in-flight branches, wherein the SBTB cache includes a FIFO having entries corresponding to each of a plurality of pipeline stages of a processor instruction pipeline~~, wherein the SBTB is included in a branch target buffer (BTB);~~

~~maintain~~ maintaining architectural branch data using a plurality of branch entries of an architectural branch target buffer (ABTB) cache coupled to the SBTB cache, the architectural branch data including the actual taken/not-taken outcomes associated with retired conditional branches, wherein the SBTB and the ABTB ~~is~~ are included in a branch target buffer (BTB) to eliminate the speculative history from the ABTB~~the BTB~~; and

~~determine~~ determining a predicted target address for a branch prediction based upon the speculative branch data and the architectural branch data, the determining of the predicted target address is performed using a target address generator coupled to the SBTB cache and the ABTB cache.

34. (Previously Presented) The method of claim 33, further comprises a fetch unit to speculatively retrieve instruction data for processing by the processor instruction pipeline.

35. (Previously Presented) The method of claim 33, wherein the SBTB cache comprises a dual-ported cache.

36. (Previously Presented) The method of claim 33, wherein the SBTB cache comprises a single-ported cache.

37. (Previously Presented) The method of claim 33, wherein the ABTB cache comprises a single-ported cache.

Claims 38-42 (Canceled)